Remarks:

Reconsideration of the application is requested.

Claims 1-11 and 16-18 remain in the application. Claims 1-5, 7, 8, 11, 18 have been amended.

In item 2 on page 2 of the Office action, claims 1-4, 7, and 16-18 have been rejected as being obvious over Simmons et al. (4,714,949) in view of Hatanaka (5,587,598) and Emori (EP 0 115 143 A2) under 35 U.S.C. § 103.

The claims have been amended to specify that an electrical connection is being produced between a first integrated circuit chip and a second integrated circuit chip. Support can be found by referring to the specification at page 15, lines 2-6, where the terms, first circuit chip and second circuit chip are used. Further, referring to the example given on page 15, lines 1-24 with reference to Fig. 2, it is clear that two integrated circuit chips are being connected. Further still, the entire disclosure is directed toward connecting two integrated circuit chips in a package. For example, see page 11, lines 23-25 with reference to Fig. 1, where it is described that the terminal pads 25, 26, 27 are connected to the pads 15, 16, 17, via bonding wires. Additional reference can be made to page 16, line 3, where chip 2 is mentioned and to page 11, line 26, where chip 1 is mentioned. It should be

clear that two separate integrated circuit chips are being connected.

The lower circuitry and the upper circuitry that the Examiner has referred to in Simmons et al. are parts of the same integrated circuit chip. Simmons et al. is directed toward increasing the yield when constructing an MIS array (column 1, lines 58-64). The described procedure involves constructing a via through the zink sulfide insulator and passivating layers to the substrate prior to forming a nickel gate structure. It should be clear that the taught process relates to the fabrication of structures on a single chip (See column 1, line 64 through column 2, line 32).

Even if there were a suggestion to combine the prior art for some reason, the invention defined by claim 1 would not have been obtained. The prior art simply does not teach or suggest a method for producing an electrical connection between two integrated circuit chips.

In item 3 on page 4 of the Office action, claims 5 and 6 have been rejected as being obvious over Simmons et al. (4,714,949) in view of Hatanaka (5,587,598) and Emori (EP 0 115 143 A2) and further in view of Kuriyama (5,682,057) under 35 U.S.C. § 103.

Claims 5 and 6 are patentable for the reasons specified above in regard to claim 1.

In item 4 on page 5 of the Office action, claims 8-11 have been rejected as being obvious over Simmons et al. (4,714,949) in view of Hatanaka (5,587,598), Kuriyama (5,682,057), Bozso et al. (5,760,478) and applicant's admitted prior art under 35 U.S.C. § 103.

Claim 8 is patentable for the reasons specified above in regard to claim 1.

Furthermore, claim 8 includes a step of disposing the surfaces of the first integrated circuit chip and the second integrated circuit chip longitudinally adjacent one another so that the first and second terminal pads of the second integrated circuit chip are not covered by the first integrated circuit chip.

The upper circuit portion and the lower circuit portion as defined by the Examiner could not be modified to be longitudinally adjacent one another, but rather are necessarily constructed one above the other.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either

show or suggest the features of claims 1 or 8. Claims 1 and 8, therefore, believed to be patentable over the art and since all of the dependent claims are ultimately dependent on claim 1 or 8, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 1-11 and 16-18 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, he is respectfully requested to telephone counsel so that, if possible, patentable language can be worked out.

Please charge any fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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GR 97 P 2681

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Albrecht Mayer

Applic. No. : 09/164,123

Filed : September 30, 1998

Title : Method for Assembling Integrated Circuits With Protection Of The Circuits Against Electrostatic Discharge, And Arragement Of Integrated Circuits With Protection Against Electrostatic Discharge

Examiner : Julio J. Maldonado

Group Art Unit : 2823

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claim 1 (twice-amended). A method for producing an electrical connection between integrated [circuits] circuit chips, which comprises:

providing a first integrated circuit chip having a terminal and a signal terminal;

forming an electrically conductive connection between the terminal and the signal terminal of the first integrated circuit chip;

providing a protective structure that becomes conductive to dissipate electrostatic discharges;

providing a second integrated circuit chip having a terminal that is coupled to the protective structure;

disposing the first integrated circuit chip and the second integrated circuit chip [and second integrated circuits] adjacent one another;

electrically connecting the signal terminal of the first integrated circuit to the terminal of the second integrated circuit chip;

connecting the terminal of the first integrated circuit chip to a terminal of a package; and

subsequent to connecting the terminal of the first integrated circuit chip to the terminal of the package, severing the electrically conductive connection between the terminal and the signal terminal of the first integrated circuit chip using an energy pulse.

Claim 2 (amended). The method according to claim 1, wherein the severing step is performed by applying an electrical current pulse to the terminal of the second integrated circuit chip.

Claim 3 (amended). The method according to claim 1, wherein the forming step includes:

forming the electrically conductive connection with a portion of reduced cross sectional area as compared to the rest of the connection; and

dimensioning the portion to dissipate electrostatic discharges between the terminal and the signal terminal of the first integrated circuit chip and to be severed during application of the energy pulse in the severing step.

Claim 4 (amended). The method according to claim 3, wherein the energy pulse used in the severing step is an electrical current pulse applied to the terminal of the second integrated circuit chip.

Claim 5 (amended). The method according to claim 1, including:

disposing the first integrated circuit chip and the second integrated circuit chip [and second integrated circuits] in a package having terminal pins so that the signal terminal of the first integrated circuit chip is not accessible from outside of the package; and

connecting the terminal of the first integrated circuit chip and the terminal of the second integrated circuit chip to a respective terminal pin of the package.

Claim 7 (amended). The method according to claim 1, wherein the disposing step is performed so that terminal of the second integrated circuit chip is not covered by the first integrated circuit chip.

Claim 8 (three-times amended). A method for producing an electrical connection between integrated [circuits] circuit chips, which comprises:

providing a first integrated circuit chip having a surface;

disposing first and second terminal pads on the surface of the first integrated circuit chip;

forming an electrically conductive connection between the first and second terminal pads of the first integrated circuit chip;

providing a second integrated circuit chip having a surface;

disposing first and second terminal pads on the surface of the second integrated circuit chip;

providing a protective structure acting as a switch that becomes conductive when there is an overvoltage to dissipate an electrostatic discharge to a line for a supply voltage;

electrically coupling at least the first terminal pad of the second integrated circuit chip to the protective structure;

disposing the surfaces of the first integrated circuit chip and the second integrated circuit chip [and second integrated circuits] longitudinally adjacent one another so that the first and second terminal pads of the second integrated circuit chip are not covered by the first integrated circuit chip;

electrically joining at least one of the first and second terminal pads of the first integrated circuit chip to one of the first and second terminal pads of the second integrated circuit chip;

severing the electrically conductive connection using an energy pulse.

Claim 11 (amended). The method according to claim 8, including electrically joining the other one of the first and second terminal pads of the first integrated circuit chip to

the other one of the first and second terminal pads of the second integrated circuit chip.

Claim 18 (amended). The method according to claim 1, which comprises performing the severing step before packaging the first integrated circuit chip and the second integrated circuit chip.